

# PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

## PCT

To:  
LARRY E. HENNEMAN JR.  
HENNEMAN & ASSOCIATES, PLC  
714 W. MICHIGAN AVE.  
THREE RIVERS, MI 49093

NOTIFICATION OF TRANSMITTAL OF  
THE INTERNATIONAL SEARCH REPORT AND  
THE WRITTEN OPINION OF THE INTERNATIONAL  
SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference 0057-014P1P	Date of mailing (day/month/year) <b>10 NOV 2008</b>
International application No. PCT/US 07/04030	International filing date (day/month/year) <b>16 February 2007 (16.02.2007)</b>
Applicant <b>TECHNOLOGY PROPERTIES LIMITED</b>	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

**Filing of amendments and statement under Article 19:**

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

**When?** The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

**Where?** Directly to the International Bureau of WIPO, 34 chemin des Colombettes  
1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

**For more detailed instructions,** see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90bis.1 and 90bis.3, respectively, before the completion of the technical preparations for international publication.

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US  
Mail Stop PCT, Attn: ISA/US  
Commissioner for Patents  
P.O. Box 1450, Alexandria, Virginia 22313-1450  
Facsimile No. 571-273-3201

Authorized officer:

*Lee W. Young*  
Lee W. Young

PCT Helpdesk: 571-272-4300  
PCT OSP: 571-272-7774

# PATENT COOPERATION TREATY

## PCT

### INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 0057-014P1P	<b>FOR FURTHER ACTION</b>	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 07/04030	International filing date ( <i>day/month/year</i> ) 16 February 2007 (16.02.2007)	(Earliest) Priority Date ( <i>day/month/year</i> ) 16 February 2006 (16.02.2006)
Applicant TECHNOLOGY PROPERTIES LIMITED		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

**1. Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

- ☒ the international application in the language in which it was filed.  
☐ a translation of the international application into \_\_\_\_\_ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

- ☒ the text is approved as submitted by the applicant.  
☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

- ☐ the text is approved as submitted by the applicant.  
☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 7  
☒ as suggested by the applicant.  
☐ as selected by this Authority, because the applicant failed to suggest a figure.  
☐ as selected by this Authority, because this figure better characterizes the invention.
- b. ☐ none of the figures is to be published with the abstract.

# INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/04030

## Box No. IV Text of the abstract (Continuation of item 5 of the first sheet)

A computer array has a plurality of computers. The computers communicate with each other asynchronously and operate in a generally asynchronous manner. When one computer attempts to communicate with another it goes to sleep until the other computer is ready to complete the transaction, thereby saving power and reducing heat production. The sleeping computer can await data or instructions. In the case of instructions, the sleeping computer waits to store the instructions or immediately execute the instructions. In the later case, the instructions are placed in an instruction register upon receipt and executed therefrom, without first placing the instructions into memory. The instructions can include a micro-loop which is capable of performing a series of operations repeatedly. In one application, the sleeping computer is awakened by an input such that it commences an action that would otherwise have required an interrupt of an otherwise active computer.

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 07/04030

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 15/00 (2008.04)

USPC - 712/221

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
USPC - 712/221Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
USPC - 712/1, 220, 221, 223 -- text search, see search terms belowElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
PubWEST(PGPB,USPT,USOC,EPAB,JPAB); Google  
Search Terms Used: instruction, register, memory, address, input, port, direct, directly, execut, jump, fetch, retriev, multipl, plural, second, increment, program counter, without, not, execute, instructions, from, ports

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 6,233,670 B1 (IKENAGA et al.) 15 May 2001 (15.05.2001), entire document especially Figs 1, 2, 5, 7, 8C; col 1, ln 42-44; col 4, ln 44-54; col 5, ln 7-15; col 6, ln 37-45, 51-65; col 7, ln 7-23.	1-4, 6-8, 10, 13, 14 ----- 5, 9, 11, 12, 15-21
Y	US 5,434,989 A (YAMAGUCHI) 18 July 1995 (18.07.1995), especially col 3, ln 13-19, 48-68; col 4, ln 1-11.	5, 11, 12, 21
Y	US 4,868,745 A (PATTON et al.) 19 September 1989 (19.09.1989), especially Figs 1, 5, 6A, 6D; col 1, ln 68; col 2, ln 6-29; col 3, ln 2-4, 6-25, 51-58; col 4, ln 6-8; col 5, ln 65-66; col 10, ln 9-14.	9, 15-20

☐ Further documents are listed in the continuation of Box C.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&amp;" document member of the same patent family

Date of the actual completion of the international search

31 October 2008 (31.10.2008)

Date of mailing of the international search report

10 NOV 2008

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents

P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774

# PATENT COOPERATION TREATY

From the  
INTERNATIONAL SEARCHING AUTHORITY

# PCT

WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

To: LARRY E. HENNEMAN JR.  
HENNEMAN & ASSOCIATES, PLC  
714 W. MICHIGAN AVE.  
THREE RIVERS, MI 49093

Date of mailing  
(day/month/year)

10 NOV 2008

Applicant's or agent's file reference  
0057-014P1P

**FOR FURTHER ACTION**

See paragraph 2 below

International application No.

PCT/US 07/04030

International filing date (day/month/year)

16 February 2007 (16.02.2007)

Priority date (day/month/year)

16 February 2006 (16.02.2006)

International Patent Classification (IPC) or both national classification and IPC

IPC(8) - G06F 15/00 (2008.04)

USPC - 712/221

Applicant **TECHNOLOGY PROPERTIES LIMITED**

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

## 2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US  
Mail Stop PCT, Attn: ISA/US  
Commissioner for Patents  
P.O. Box 1450, Alexandria, Virginia 22313-1450  
Facsimile No. 571-273-3201

Date of completion of this opinion

31 October 2008 (31.10.2008)

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300  
PCT OSP: 571-272-7774

WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US 07/04030

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
  - ☒ the international application in the language in which it was filed.
  - ☐ a translation of the international application into \_\_\_\_\_ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
  - a. type of material
    - ☐ a sequence listing
    - ☐ table(s) related to the sequence listing
  - b. format of material
    - ☐ on paper
    - ☐ in electronic form
  - c. time of filing/furnishing
    - ☐ contained in the international application as filed
    - ☐ filed together with the international application in electronic form
    - ☐ furnished subsequently to this Authority for the purposes of search
4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US 07/04030

Box No. V	Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement																								
<p><b>1. Statement</b></p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td rowspan="2" style="width: 30%; vertical-align: top;">Novelty (N)</td> <td style="width: 15%;">Claims</td> <td style="width: 40%; border-bottom: 1px solid black;">5, 9, 11, 12, 15-21</td> <td style="width: 15%; text-align: right;">YES</td> </tr> <tr> <td>Claims</td> <td style="border-bottom: 1px solid black;">1-4, 6-8, 10, 13, 14</td> <td style="text-align: right;">NO</td> </tr> <tr> <td rowspan="2" style="vertical-align: top;">Inventive step (IS)</td> <td>Claims</td> <td style="border-bottom: 1px solid black;">None</td> <td style="text-align: right;">YES</td> </tr> <tr> <td>Claims</td> <td style="border-bottom: 1px solid black;">1-21</td> <td style="text-align: right;">NO</td> </tr> <tr> <td rowspan="2" style="vertical-align: top;">Industrial applicability (IA)</td> <td>Claims</td> <td style="border-bottom: 1px solid black;">1-21</td> <td style="text-align: right;">YES</td> </tr> <tr> <td>Claims</td> <td style="border-bottom: 1px solid black;">None</td> <td style="text-align: right;">NO</td> </tr> </table>					Novelty (N)	Claims	5, 9, 11, 12, 15-21	YES	Claims	1-4, 6-8, 10, 13, 14	NO	Inventive step (IS)	Claims	None	YES	Claims	1-21	NO	Industrial applicability (IA)	Claims	1-21	YES	Claims	None	NO
Novelty (N)	Claims	5, 9, 11, 12, 15-21	YES																						
	Claims	1-4, 6-8, 10, 13, 14	NO																						
Inventive step (IS)	Claims	None	YES																						
	Claims	1-21	NO																						
Industrial applicability (IA)	Claims	1-21	YES																						
	Claims	None	NO																						
<p><b>2. Citations and explanations:</b></p> <p>Claims 1-4, 6-8, 10, 13 and 14 lack novelty under PCT Article 33(2) as being anticipated by US 6,233,670 B1 to Ikenaga et al. (hereinafter 'Ikenaga').</p> <p>Regarding claim 1, Ikenaga discloses in a computer for executing a series of instructions (Figs 1, 7; col 4, ln 52-54), an improvement comprising: an instruction register for temporarily storing a group of instructions to be executed (Fig 1 and col 4, ln 44-47 -- e.g., one of improved function units 4, 5, 6, and 7); and a program counter for storing an address from which a group of instructions is retrieved into said instruction register (Figs 1, 7; col 1, ln 42-44; col 4, ln 52-54); wherein the address in said program counter can be either a memory address or the address of a register (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1).</p> <p>Regarding claim 2, Ikenaga further discloses wherein: the address in said program counter can, optionally, point to a plurality of registers (Figs 1, 8C and col 6, ln 59-65 -- e.g., to function units 4 and 5).</p> <p>Regarding claim 3, Ikenaga further discloses wherein: said group of instructions includes more than one instruction (Fig 8C and col 6, ln 59-65 -- e.g., instructions 11 and 12).</p> <p>Regarding claim 4, Ikenaga further discloses wherein: when there are no instructions left to be executed in the instruction register then the computer will fetch an instruction group according to the address stored in the program counter (Fig 8C and col 1, ln 42-44 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter).</p> <p>Regarding claim 6, Ikenaga further discloses wherein: when an instruction in said group of instructions is a jump instruction (Fig 8C and col 7, ln 7-23 -- bypass), then the program counter is loaded with an address indicated by the jump instruction (col 7, ln 7-23).</p> <p>Regarding claim 7, Ikenaga further discloses wherein: the address indicated by the jump instruction follows the jump instruction in the group of instructions (Figs 1, 8C; col 6, ln 63-65 and col 7, ln 7-23 -- e.g., the address and the instruction associated with function units that follow each other such as function units 4 and 5).</p> <p>Regarding claim 8, Ikenaga discloses a method for executing instructions in a computer, (Figs 1, 7; col 4, ln 52-54) comprising: (a) fetching a group of instructions from an address (Fig 1 and col 4, ln 44-47 -- instruction fetching stage 2), wherein the address can be either an address of a memory location or an address of a port (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1); (b) placing said group of instructions in an instruction register to be executed (Fig 1 and col 4, ln 44-54 -- e.g., placing in one of improved function units 4, 5, 6, and 7); and (c) executing at least one of said group of instructions from said instruction register (Fig 8C and col 6, ln 51-64).</p> <p>Regarding claim 10, Ikenaga further discloses wherein: when all of the instructions in the instruction group have been executed then yet another group of instructions is fetched (Fig 8C and col 1, ln 42-44 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter).</p> <p>Regarding claim 13, Ikenaga further discloses: in step (c) either executing all instructions in said group of instructions or else executing the instructions in said group of instructions until a diversion instruction is encountered (Fig 8C and col 7, ln 7-23 -- e.g., executing until a bypass occurs); wherein said diversion instruction is an instruction that provides for fetching a group of instructions from yet another location (col 6, ln 63-65 and col 7, ln 7-23 -- e.g., data executed in the other pipeline PL1 is applied; Fig 2 and col 6, ln 51-57 -- fetching stage 2).</p> <p>Regarding claim 14, Ikenaga further discloses wherein: the diversion instruction is a JUMP instruction (Fig 8C and col 7, ln 7-23 -- bypass).</p> <p style="margin-top: 20px;">-- See Supplemental Box --</p>																									

WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US 07/04030

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:  
Box No. V.2. Citations and explanations:

Claims 5, 11, 12 and 21 lack an inventive step under PCT Article 33(3) as being obvious over Ikenaga in view of US 5,434,989 A (Yamaguchi).

Regarding claim 5, Ikenaga teaches the computer of claim 1 and further discloses that: when the computer retrieves a group of instructions from a memory, then the program counter is incremented (Fig 8C; col 1, ln 42-44 and col 5, ln 7-9 -- e.g., when instructions 11 and 12 have both been fully executed, another group of instruction is retrieved based on the address signal generated from the program counter such as from source addresses SA1 and SA2). Ikenaga does not expressly disclose that: when the computer retrieves a group of instructions from a register, then the program counter is not incremented. However, Yamaguchi does teach that: when the computer retrieves a group of instructions from a register, then the program counter is not incremented (col 3, ln 48 to col 4, ln 11 -- e.g., by utilizing an address type of a third or fourth type said types not associated with incrementing the program counter). It would have been obvious to one of ordinary skill in the art to modify the computer of Ikenaga so as to not increment the program counter as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from computers configured to not increment the address if the address is that of a port, because such computers can be implemented using multiple types of address types, thereby increasing the flexibility of the design to the particular application of interest to the designer (Yamaguchi col 3, ln 48 to col 4, ln 11).

Regarding claim 11, Ikenaga teaches the method of claim 10 and further discloses that if the address is the address of a memory location, then the address is incremented before the yet another group of instructions is fetched (Fig 8C; col 1, ln 42-44 and col 5, ln 7-9 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter such as from source addresses SA1 and SA2). Ikenaga does not expressly disclose that if the address is the address of a port, then the address is not incremented before the yet another group of instructions is fetched. However, Yamaguchi does teach that if the address is the address of a port, then the address is not incremented before the yet another group of instructions is fetched (col 3, ln 48 to col 4, ln 11 -- e.g., by utilizing an address type of a third or fourth type said types not associated with incrementing the program counter). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to not increment the address before fetching another group of instructions if the address is that of a port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from methods that do not increment the address if the address is that of a port, because such methods can be implemented using multiple types of address types, thereby increasing the flexibility of the method to the particular application of interest to the designer (Yamaguchi col 3, ln 48 to col 4, ln 11).

Regarding claim 12, Ikenaga teaches the method of claim 8 but does not expressly disclose that the address can indicate more than one port. However, Yamaguchi does teach that the address can indicate more than one port (col 3, ln 13-19). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to utilize an address that can indicate more than one port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from methods that utilize addresses that can indicate more than one port, because such methods can be used in dual port memory arrays (Yamaguchi col 3, ln 13-19).

Regarding claim 21, Ikenaga discloses a computer for executing a series of instructions (Figs 1, 7; col 4, ln 52-54), the computer comprising: an instruction register for temporarily storing a group of instructions (Fig 1 and col 4, ln 44-47 -- e.g., one of improved function units 4, 5, 6, and 7); a logic unit for executing the instructions stored in said instruction register (Fig 5 and col 6, ln 37-45); and means for fetching the group of instructions into said instruction register (Fig 1 and col 4, ln 44-47 -- instruction fetching stage 2). Ikenaga does not expressly disclose fetching from a port. However, Yamaguchi does teach fetching from a port (col 3, ln 13-19). It would have been obvious to one of ordinary skill in the art to modify the computer of Ikenaga so as to fetch from a port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from computers with instructions for fetching from a port, because such computers can incorporate dual port memory arrays (Yamaguchi col 3, ln 13-19).

Claims 9 and 15-20 lack an inventive step under PCT Article 33(3) as being obvious over Ikenaga in view of US 4,868,745 A to Patton et al. (hereinafter 'Patton').

Regarding claim 9, Ikenaga teaches the method of claim 8 but does not expressly disclose that the address is retrieved from a program counter register. However, Patton does teach that the address is retrieved from a program counter register (col 3, ln 51-58 and col 4, ln 6-8 -- e.g., from a prologue in the immobile code area; Fig 6D and col 10, ln 9-14). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to retrieve the address from a program counter register as taught by Patton, because Ikenaga and Patton are directed to systems and methods for executing instructions and processing data with a minimum of processing steps. Furthermore, designers benefit from methods that execute instructions using an address retrieved from a program counter register, because such methods allow for intermixing data, pointers and instructions to be executed directly or indirectly (Patton col 2, ln 6-29).

-- See next Supplemental Box --



WRITTEN OPINION OF THE  
INTERNATIONAL SEARCHING AUTHORITY

International application No.  
PCT/US 07/04030

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:  
Box No. V.2. Citations and explanations:

Regarding claim 15, Ikenaga discloses a method for handling data blocks in a computer (Figs 1, 7; col 4, ln 52-54; Fig 8C and col 6, ln 52-65 -- e.g., data blocks comprising instructions 11 and 12), comprising: (a) fetching a data block from an address (Fig 1 and col 4, ln 44-47 -- instruction fetching stage 2; Fig 8C -- e.g., a data block comprising instruction 11, instruction 12, or both), wherein the address can be either an address of a memory location or an address of a port (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1); and (b) if said data block contains a group of instructions then providing said data block to an instruction register (Fig 8C and col 6, ln 59-65 -- e.g., providing instruction 11 and 12 to function units 4 and 5). Ikenaga further discloses that (c) if said data block contains data then providing said data block to the top of a data stack (Fig 2 and col 5, ln 7-15 -- e.g., data comprising SA1, SA2 and DA). Ikenaga does not expressly disclose that the data block contains data rather than instructions. However, Patton does teach that the data block contains data rather than instructions (Fig 1 and col 3, ln 2-4; col 1, ln 68, col 2, ln 6-10 and col 3, ln 24-25 -- e.g., objects for direct object execution comprising data but no OPs). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to utilize a data block that contains data rather than instructions as taught by Patton, because Ikenaga and Patton are directed to systems and methods for executing instructions and processing data with a minimum of processing steps. Furthermore, designers benefit from methods that process data alone, because such methods allow for direct or indirect execution or processing regardless of the nature of the intermixed data, pointers and instructions (Patton col 2, ln 6-29).

Regarding claim 16, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses wherein: said group of instructions can, optionally, also contain data (col 5, ln 7-9).

Regarding claim 17, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses wherein: the question of whether said data block contains a group of instructions or data is determined by whether the last instruction in a previous group of instructions has been executed (Fig 8C and col 5, ln 7-9 -- e.g., when a previous group comprising instructions 11 and 12 has been executed, decoding stage 3 obtains a new instruction comprising first an instruction code OP; col 7, ln 14-23 -- e.g., and when instructions 11 and 12 have not yet been fully executed, data is transmitted through bypass line 12).

Regarding claim 18, Ikenaga and Patton teach the method of claim 17. Ikenaga further discloses wherein: when the last instruction in said previous group of instructions has been executed then it is determined that the data block contains a group of instructions (Fig 8C and col 5, ln 7-9 -- e.g., when a previous group comprising instructions 11 and 12 has been executed, decoding stage 3 obtains a new instruction that includes an instruction code OP).

Regarding claim 19, Ikenaga and Patton teach the method of claim 15. Patton further discloses wherein: the data stack is a primary data stack (Fig 6A -- P4, P5; Fig 5 and col 3, ln 6-23 and col 5, ln 65-66 -- e.g., primary and sole data stack in the data processing system of Fig 5).

Regarding claim 20, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses that if said data block contains a group of instructions, then executing instructions from said group of instructions from the instruction register (Fig 8C and col 6, ln 51-65).

Claims 1-21 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.